## WHAT IS CLAIMED IS:

1	1. An output stage comprising:
2	a p-channel inverter device coupled to a first supply voltage;
3	a p-channel stacked device coupled between the p-channel inverter and a pad;
4	an n-channel stacked device coupled to the pad; and
5	an n-channel inverter device coupled between the n-channel stacked device and a
6	second supply,
7	wherein a gate of the p-channel stacked device receives a first bias voltage and a
8	gate of the n-channel stacked device receives a second bias voltage, and the first bias voltage and
9	the second bias voltage vary depending on a voltage difference between the first supply voltage
10	and the second supply voltage.
1	2. The output stage of claim 1 further comprising:
2	a first voltage translator coupled to a gate of the p-channel inverter device,
3	wherein the first voltage translator translates a signal in a first voltage range to a second voltage
4	range, the second voltage range defined by the first supply voltage and the second supply
5	voltage.
1	3. The output stage of claim 2 further comprising:
2	a second voltage translator coupled to a gate of the n-channel inverter device,
3	wherein the second voltage translator translates a signal in the first voltage range to the second
4	voltage range.
1	4. The output stage of claim 3 wherein the second supply voltage is ground.
1	5. The output stage of claim 1 wherein the output stage is tri-stated by setting
2	the first bias voltage approximately equal to the first supply voltage and the second bias voltage
3	approximately equal to the second supply voltage.
1	6. The output stage of claim 5 wherein the n-channel stacked device receives
2	the first bias voltage at its gate, and the p-channel stacked device receives the second bias
3	voltage at its gate

l	7. The output stage of claim 5 wherein when the voltage difference between
2	the first supply voltage and the second supply voltage is approximately equal to the sum of the
3	drain-to-source breakdown voltages for the p-channel and n-channel inverter devices, the first
4	bias voltage and the second bias voltage are approximately equal and near the mid-point between
5	the first supply voltage and the second supply voltage.
1	8. The output stage of claim 7 wherein the bulk of the p-channel stacked
2	device is coupled to a body bias circuit, and
3	wherein the body bias circuit generates a voltage that tracks the higher voltage
4	between the first supply voltage and a received voltage.
1	9. An integrated circuit comprising:
2	an input stage coupled to a pad;
3	an output stage coupled to the pad; and
4	a bias circuit coupled to the pad
5	wherein the output stage comprises a first p-channel device coupled to the pad,
6	the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is
7	connected to the bias circuit, and
8	wherein the gate of the first p-channel device receives a first bias voltage, and the
9	first bias voltage is selected based on a supply voltage received by the output stage.
1	10. The integrated circuit of claim 9 wherein the output stage further
2	comprises:
3	a second p-channel device coupled to receive the supply voltage and further
4	coupled to the first p-channel device.
1	11. The integrated circuit of claim 10 wherein the output stage further
2	comprises:
3	a first n-channel device coupled to the first p-channel device, the first n-channel
4	device comprising a gate,
5	wherein the gate of the first n-channel device receives a second bias voltage, and
6	the second bias voltage is selected based on a supply voltage received by the output stage.

1	12. The integrated circuit of claim 10 further comprising:
2	a first voltage translator coupled to a gate of the first p-channel device, wherein
3	the first voltage translator translates a signal in a first voltage range to a second voltage range,
4	the second voltage range defined by the first supply voltage and a second supply voltage,
5	wherein the second supply voltage is ground.
1	13. An integrated circuit comprising:
2	an input stage coupled to a pad;
3	an output stage coupled to the pad and receiving a first power supply; and
4	a bias circuit coupled to the pad
5	wherein the output stage comprises a first p-channel device coupled to the pad,
6	the first p-channel device comprising a bulk, a drain, a gate, and a source, and the bulk is
7	connected to the bias circuit, and
8	wherein the bias circuit comprises a first device and a second device coupled in
9	series between the pad and the bulk of the first p-channel device, the first device biased to protect
10	the second device from voltages on the pad.
1	14. The integrated circuit of claim 13 wherein a gate of the second device is
2	coupled to the first power supply.
۷	coupled to the first power supply.
1	15. The integrated circuit of claim 14 wherein a gate of the first device is
2	coupled to a bias voltage, the bias voltage set to protect the first device from voltages on the pad.
1	16. The integrated circuit of claim 13 wherein the first device and the second
2	device are p-channel devices.
1	17. The integrated circuit of claim 13 wherein the output stage further
2	comprises:
3	a second p-channel device coupled to receive the first supply voltage and further
4	coupled to the first p-channel device, wherein the bulk of the first p-channel device is coupled to
5	the bulk of the second p-channel device.
1	18. The integrated circuit of claim 17 further comprising:

- a first voltage translator coupled to a gate of the first p-channel device, wherein
  the first voltage translator translates a signal in a first voltage range to a second voltage range,
  the second voltage range defined by the first supply voltage and a second supply voltage,
  wherein the second supply voltage is ground.
  - 19. The integrated circuit of claim 13 wherein the first p-channel device receives a bias voltage at its gate, and the bias voltage is determined by the first supply voltage.
- 1 20. The integrated circuit of claim 19, wherein the integrated circuit is a 2 programmable logic device.

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